

## CMC206 Trigger Control Program

This module accepts as inputs a Gate signal, and Busy signals (from the DAQ modules triggered by the Gate). The Nim and ECL Gate signals are OR'd together to make one Gate. The ECL and Nim busy input signals are also OR'd together.

The outputs are the Gate signal, both as Nim and ECL, and a Busy signal.

The Gate signal can be the same width as the incoming gate (width register = 0) or can be reshaped with the width determined by the 10 bit width register.

Without reshaping, the output width is exactly the same as the input width, delayed by about 25 ns. When reshaping is used, the input width is not important, only the leading edge is used. The Gate output width is very precise, but, the time of the leading edge is delayed by 35 ns, and the leading edge jitters over a 5 ns range (from 35 – 40 ns).

The LSB is 5 nS, so the maximum gate width is about 5 microseconds. There is 10 nS added to the width from the register so the width is:

Width Register	Output Gate Width (5 nS LSB)
0	same as input
1	15 ns
2	20 ns
100	510 ns
1000	1010 ns
1023	5125 ns

The Busy period, or dead time can be determined by two methods. If the dead time register is 0, then the Gates are blocked (no further Gate outputs allowed) starting at the leading edge of the input Gate, ending when the OR of the busy inputs becomes True (at least one busy input) and then becomes false (end of busy). If no busy signal ever arrives, the Gate will remain blocked.

If the dead time register is non zero, the dead time is fixed, using the value in the register (LSB = 1 microsecond). The register is 12 bits, so the maximum fixed dead time is 4.095 milliseconds. The busy inputs are ignored, the dead time is completely fixed by the register contents (1 microsecond LSB).

The DAQ system is started by loading the dead time and width registers as desired, clearing the counters with f9 A0, then enabling with F26 A0. Now the system will pass gates to the output.

To stop the system, disable the gates with F24 A0.

There are two 48 bit counters that measure the total time between the enable and disable commands, and the dead time (when the gates are blocked). These counters count a 1 MHz clock. The total system live time is just the difference between the two counters.

## CMC206 Trigger Control Program

### Pin assignments

C0 ECL Busy input  
C1 ECL Busy input  
C2 ECL Busy input  
C3 ECL Busy input  
C4 ECL Busy input  
C5 ECL Busy input  
C6 ECL Busy input  
C7 ECL Busy input  
C8 ECL Busy input  
C9 ECL Busy input  
C10 ECL Busy input  
C11 ECL Busy input

C12 ECL Gate input

Nim0 Nim Gate input

Nim1 Nim Gate Output

Nim2 Nim Gate Output

Nim3 Nim Busy input

Nim4 Nim Busy input

Nim5 Nim Busy input

Nim6 Nim Busy Output

B0 ECL Gate Output

B1 ECL Gate Output

B2 ECL Gate Output

B3 ECL Gate Output

B4 ECL Gate Output

B5 ECL Gate Output

B6 ECL Gate Output

B7 ECL Gate Output

B8 ECL Gate Output

B9 ECL Gate Output

B10 ECL Gate Output

B11 ECL Gate Output

B12 ECL Gate Output

B13 ECL Gate Output

B14 ECL Gate Output

B15 ECL Gate Output

B16 ECL Gate Output

A0-16 are not used (rear panel)

### Camac Commands

F0 A0 read dead time register  
F0 A1 read gate width register  
F0 A4 read memory address  
F0 A5 read memory (LS 24 bits of 32)  
F0 A6 read last command, ZCIFA (12 bits)  
F0 A8 read memory (mS 24 bits of 32)  
F0 A9 read firmware version number  
  
F1 A0 read LS 24 bits of total time enabled  
F1 A1 read MS 24 bits of total time enabled  
F1 A2 read LS 24 bits of Dead time  
F1 A3 read MS 24 bits of Dead time  
  
F9 A0 clear total time and dead time counters  
  
F16 A0 write dead time register (12 bits)  
F16 A1 write gate width register (10 bits)  
F16 A4 write memory address (20 bits)  
F16 A5 write memory (LS 24 bits of 32)  
F16 A8 write memory (mS 24 bits of 32)  
  
F24 A0 Disable Gates  
F26 A0 Enable Gates  
F27 A0 Test Gate Enable (Q=1 if enabled)

Note: Z or C clears everything